CLAIMS

In the Claims:

Claims 1-20 are pending.

Please **AMEND** claims 1 and 8 as shown below.

A complete listing of the claims and a status of each is provided as follows.

1. (Currently Amended) A memory system having a reduced refresh rate in a sleep mode, comprising:

a dynamic memory;

an error correction code (ECC) memory allocation circuit for identifying non-critical bit addresses in said dynamic memory and allocating said addresses as ECC addresses when entering from an active mode to sleep mode;

an ECC encoder for encoding critical bits with error correction codes, said error correction codes being stored in said ECC addresses;

a refresh execution circuit for reducing [[said]] a refresh rate in said sleep mode and increasing said refresh rate in said active mode; and

an ECC decoder for decoding said critical bits encoded with said error correction codes when reentering said active mode.

2. (Original) A memory system as recited in claim 1 further comprising a storage device for storing sleep mode refresh rate data.

3. (Original) A memory storage device as recited in claim 2 wherein said storage device comprises a fusible link.

4. (Original) A memory system as recited in claim 1 further comprising:

a storage device for storing a plurality of sleep mode refresh rate data; and

a temperature sensor, wherein said refresh execution circuit selects one of said sleep mode refresh rate data according to operating temperature.

5. (Original) A memory system as recited in claim 4 wherein said storage device comprises a fusible link.

6. (Original) A memory system as recited in claim 4 wherein said refresh rate is reduced by a 2X factor for each decade Celsius reduction in operating temperature.

7. (Previously Presented) A memory system as recited in claim 1 wherein said error correction codes comprise one of Reed-Solomon code and Bose-Chaudhuri-Hocquenghem code.

8. (Currently Amended) A memory system as recited in claim 1 wherein said ECC memory allocation circuit ~~stores preallocated~~ reassigns said non-critical bit addresses ~~in said dynamic~~ as a second memory space designated for storing ECC parity bits.

9. (Original) A memory system as recited in claim 1 wherein said ECC memory allocation assigns ECC addresses dynamically to the last byte of each word address.

10. (Original) A method for reducing the refresh rate of a memory in sleep mode, comprising the steps of:

switching from an active mode to a sleep mode;

identifying non-critical bit addresses;

encoding critical bits with an error correction code (ECC);

storing ECC codes at said non-critical bit addresses;

reducing a refresh rate for said memory;

performing error correction on said critical bits using said ECC codes when reentering active mode; and

discarding said ECC bits.

11. (Original) A method for reducing the refresh rate of a memory in sleep mode as recited in claim 10 further comprising the steps of:

determining an operating temperature for said memory; and

selecting one of a plurality of refresh rates based on said operating temperature of said memory.

12. (Original) A method for reducing the refresh rate of a memory in sleep mode as recited in claim 11 further comprising the step of:

reducing said operating temperature by a 2X factor for each decade Celsius reduction in operating temperature.

13. (Original) A method for reducing the refresh rate of a memory in sleep mode as recited in claim further comprising the step of:

preallocating addresses in memory to store non-critical bits.

14. (Original) A method for reducing the refresh rate of a memory in sleep mode as recited in claim 10 further comprising the step of:

storing said ECC codes for a word of a last byte address for said word.

15. (Original) A computer readable medium embodying instructions for causing a computer to take steps to reduce the refresh rate of a memory in sleep mode, the steps comprising:

switching from an active mode to a sleep mode;

identifying non-critical bit addresses;

encoding critical bits with an error correction code (ECC);

storing ECC codes in said non-critical bit addresses;

reducing a refresh rate for said memory;

performing error correction on said critical bits using said ECC codes when reentering active mode; and

discarding said ECC bits.

16. (Original) A computer readable medium embodying instructions for causing a computer to take steps to reduce the refresh rate of a memory in sleep mode as recited in claim 15, the steps further comprising:

reducing said operating temperature by a 2X factor for each decade Celsius reduction in operating temperature.

17. (Original) A computer readable medium embodying instructions for causing a computer to take steps to reduce the refresh rate of a memory in sleep mode as recited in claim 15, the steps further comprising:

preallocating addresses in memory to store non-critical bits.

18. (Original) A computer readable medium embodying instructions for causing a computer to take steps to reduce the refresh rate of a memory in sleep mode as recited in claim 15, the steps further comprising:

storing said ECC codes for a word of a last byte address for said word.

19. (Original) A computer readable medium embodying instructions for causing a computer to take steps to reduce the refresh rate of a memory in sleep mode as recited in claim 15 wherein said error correction codes comprise Reed-Solomon code.

20. (Original) A computer readable medium embodying instructions for causing a computer to

take steps to reduce the refresh rate of a memory in sleep mode as recited in claim 15, wherein said error correction codes comprise Bose-Chaudhuri-Hocquenghem code.